International
Manufacturing
Services, Inc.

Supplied in separate documents are modeled S-parameters for various 50 ohm IMS chip resistors of "PW" design.

Please keep in mind the following assumptions that must be accounted for when creating or using s-parameters for a given device, whether modeled or tested:

1] chip is mounted in a 50 ohm system

2] 50 ohm system is matched

3] output of chip is assumed to be grounded (for S11 data), so that the model represents a 50 ohm chip ***at the end*** of a 50 ohm system.

4] for each chip, a series inductance (provided by customer mounting) is assumed and a capacitance is calculated. These capacitance values represent the series and parallel cap's which are inherent to the device and the assumed mounting techniques employed for the device when it is mounted in a 50 ohm system.

5] these "PW" chips are designed to be mounted face down on a 50 ohm substrate line. If mounted face up, then the ideal mounting technique would include ensuring that the resistor (on top of the chip) and the incoming transmission line are in the same plane. Otherwise a significant mismatch occurs (due to a discontinuity between the chip and the incoming microstrip line), the magnitude of which is dependent on the nature of the mismatch and the frequency of operation.

As with any model, or even with real tests, the resulting data is always particular to the fixture and/or system into which the chip is mounted (or particular to the ***assumptions*** about that fixture mounting, when modeled). Therefore, the data will likely not reflect the actual performance of the device when physically mounted into your circuit, as there are many variables that are beyond the control of anyone other than the actual user.

In addition, since there are many different implementations of a 50 ohm system (into which the chip will presumably be mounted), the resulting performance will really depend on the nature of that system and the user's ability to "tune" the chip into it. (for instance, a 50 ohm system on FR4, or Rogers Duroid or alumina will have different geometries depending on the system, which will cause different reactances to manifest themselves once the chip is mounted in that system)

For the above reasons, a second example of s parameters is provided for the 0502 chip, where the mounting capacitances (due to customer mounting) are assumed to be a different value (than with the 1st set). Note that the larger capacitance (2nd set labelled 0502B) causes a larger S11 magnitude.

please contact IMS with any questions.

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